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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,200	03/14/2001	William P. Moore	BU9-98-050DIV1	2598

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/805,200	MOORE ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *appeal brief filed 4/14/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,9,20 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,9,20 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 4/14/05, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

2. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

3. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

4. The rejections of claims 1-4,9,20,23-29 are maintained and repeated below. However a new rejections on claims 6 and 30 are set forth below.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Damouny (4,713,750).

7. In regard to claim 20, Damouny discloses a method of providing a state machine decoding, comprising:

a. decoding a current opcode to provide a decode; [Column 3, lines 41-49 and column 4, lines 30-35 show an opcode is mapped or decoded.]

b. setting required functions signals; [This section also shows that the pointers are necessary for execution and thus are required function signals]

c. setting exclusive functions outside of the current opcode to a previous state; [Column 18, lines 1-8 show that pointer generated by previous instructions (outside the current opcode) pass through other latches, thus functionally setting these exclusive DODA and EXEC latches to a previous state (due to the previous instructions)]

d. and latching results of the decode. [Column 4, lines 35-38 show that the pointers resulting from a decode are stored in a latch.]

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 9, and 23-29 are under rejected under 35 U.S.C. 103(a) as being unpatentable over Damouny in view of Thoma (patent No. 4,484,268).

In regard to claim 1,

a. Damouny discloses a microprocessor, comprising: a microcode unit (figure 1A, element 54) for outputting control signals (element 182), for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode comprising:

i. an instruction address input for receiving an instruction address; [Figure 1A shows that element 156 (and thus the microcode unit) receives addresses on an input via line 168, which is output element 164, for the next microaddress or microinstruction address.]

ii. a control variable input for receiving a control variable corresponding to a current state of the microprocessor; [Figure 1A shows that the microcode unite has a control variable input 184. Column 4, lines 57-61 show that the input signals received on bus 184 correspond to and control the internal state.]

iii. a control signal input for receiving all the controls signals output by the microcode unit for an immediately preceding instruction; [Figure 1A shows that element 180 (and thus the microcode unit receives on an input the control signal 182, which is output by element 164 and thus the microcode unit. Column 4, lines 57-61 show that this signal 182 is an control signal. Column 18, lines 1-8, show that the signal on bus 182 is generated in previous instructions and supplied in a next cycle.]

iv. an embedded logic circuit dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction. [Figure 1A shows an embedded logic PLA circuit 180 that decodes branch conditions for branch instructions. Column 4, lines 53-61 show that this branch PLA generates the control for selecting the NMA or next microaddress based on branch conditions and thus evaluates branch instructions (a unique type of instruction). As shown in figure 1A, the branch PLA's 180 are responsive to the control variable (element 184) , the control signals for an immediately preceding instruction (element (182) , and to the table lookup for setting the required control signals (element 183).]

b. Damouny does not disclose a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

c. Thoma has disclosed in figure 1 the use of multiple PLA embedded logic circuits. Circuits 2, lines 6-9 show that each PLA is optimized for decoding a given instruction class (or evaluating a unique instruction type).

d. The background section of Thoma shows that prior art PLA decoding using only one PLA results in physically large design and performance degradation manifest in slower machine speeds. The

summary shows that the improvement is in using multiple PLA's and thus this performance degradation is avoided. This ability to have a better performing or faster machine would have motivated one of ordinary skill in the art to modify the design of Damouny to use multiple PLA's for evaluating unique instruction types as taught by Thoma. With this methodology in place in the disclosure of Damouny, multiple PLA's would be used in place of the single branch PLA so that a PLA that is too large is avoided and no performance degradation occurs.

10. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Damouny to use multiple PLA's, as taught Thoma, in place of the single branch PLA so that increased speed in the processing machine may be realized.

In regard to claim 2, Damouny in view of Thoma discloses the microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a. table for performing a table lookup in response to a received instruction; [A PLA inherently uses a table. As reference of this inherency, the Hennessy (Computer Archiecture) textbook explicity shows on pages 205-206 that a PLA is a table with entries for lookup. In addition, Hennessy (Computer Organization and Design) has shown on pages B-11 to B-13 that PLA includes a pair of table, and AND plane and an OR plane. These tables are used to perform table lookups because the inputs into the AND table are transformed into intermediate values that

fall down or the OR table and get further transformed into what results as the outputs.]

b. and a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction. [As shown in figure 1A of Damouny, the branch PLA's 180 are responsive to the control variable (element 184), the control signals for an immediately preceding instruction (elements 182) and to the table lookup for setting the required control signals (element 183). The tables use the control signals input to lookup the control signals to be output to element 156 via line 183.]

11. In regard to claim 3, Damouny discloses the microprocessor of claim 2, wherein the controller includes:

a. means for setting a control signal to a "1" regardless to its immediately preceding value;

b. means for setting a control signal to a "0" regardless of its immediately preceding value;

c. and means for not modifying a control signal from its immediately preceding value.

[Column 3, lines 14-17 show that the control signals are set to active high ("1") and active low ("0"). Since limitations (a) and (b) of the claim state that this setting is regardless of the preceding value, the value may or may not (regardless) be set based on previous and thus these limitations are met since

all that is required is the setting of the control signals to a "1" and to a "0". When the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value.]

12. In regard to claim 4, Damouny discloses the microprocessor of claim 3, wherein the controller includes: means for setting a control signal to a data state. [As shown above, the control signals are set to active low or active high a "0" or a "1" respectively Since a "1" or "0" bit is data, the control is set to a data state.]

13. In regard to claim 9,

a. Damouny discloses a microcode unit a microprocessor (figure 1A, element 54) for outputting control signals (element 182), for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode comprising:

i. an instruction address input for receiving an instruction address; Figure 1A shows that element 156 (and thus the microcode unit) receives addresses on an input vial line 168, which is output by element 164, for the next micro address or microinstruction address .]

ii. a control variable input for receiving a control variable corresponding to a current state of the microprocessor; [Figure 1A show that the microcode unit has a control variable input 184. Column 4, lines 57-61 show that the input signals received on bus 184 correspond to and control the internal state.]

iii. a control signal input for receiving all the control signals output by the microcode for an immediately preceding instruction; (Figure 1A shows that element 180 (and thus the microcode unit receives on an input the control signal 182, which is output by element 164 and thus the microcode unit. Column 4, lines 57-61 show that this signal on bus 182 is generated in previous instructions and supplied in a next cycle.]

iv. And an embedded logic circuit dedicated for evaluating types of instructions received by the microcode unit and for setting the control signals required for executing said receiving instruction. [Figure 1A shows a PLA element 150 that maps instructions or decodes opcodes. Column 4, line 30-61 show that this mapping generates pointers necessary for execution and address calculation and thus the instructions are evaluated to generated these pointers. Column 3, lines 41-49 show that this one unit maps or evaluates for each instruction given in Appendix B. As shown in figure 1A, the branch PLA's 180 are responsive to the control variable (element 184), the control signals for an immediately preceding instruction (element 182), and to the table lookup for setting the required control signals (element 183).]

b. Damouny does not disclose a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

c. Thoma has disclosed in figure 1 the use of multiple PLA embedded logic circuits. The summary shows that the PLA's decode the opcodes of instructions. Column 2, lines 6-9 show that each PLA is optimized for decoding a given instruction class (or evaluating a unique instruction type).

d. The background section of Thoma shows that prior art PLA decoding using one PLA result in physically large design and performance degradation manifest in slower machine speeds. The Summary shows that the improvement is in using multiple PLA's and thus this performance degradation is avoided. This ability to have a better performing or faster machine would have motivated one of ordinary skill in the art to modify the design or Damouny to use multiple PLA's for opcode decoding as taught by Thoma.

14. It would have been obvious to one or ordinary skill in the art at the time of invention to modify the design of Damouny to include multiple PLA's as taught by Thoma so that increased speed in the processing machine may be realized.

15. In regard to claim 23, Damouny in view of Thoma disclose microprocessor of claim 1, wherein each plurality of embedded logic circuits comprises a controller for controllably setting each of the control signals required by the microprocessor for executing said received instruction [As shown in figure 1A, branch PLA's 180 are responsive to the control variable (184), the control signals for immediately preceding instruction (element 182), and table lookup for setting the required control signals (element 183).]

16. In regard to claim 24, Damouny in view of Thoma disclose the microprocessor of claim 1, wherein each plurality of embedded logic circuits comprises a controller for controllably setting each of the control signals required by the microprocessor for executing said received instruction [As shown in figure 1A, branch PLA's 180 are responsive to the control variable (184), the control signals for immediately preceding instruction (element 182), and table lookup for setting the required control signals (element 183).] One can see the added stipulation of "only" is met by the following example. In an example if a control word from PLA table is "11 0000 0000 00 0000 0010 000" (as is the first output entry from the PLA in appendix B), the necessary bits that must be set to "1" are bits 4, 21, and 22 (with zero being the first bit on the right) and these are the *only* bits set to a 1 in the control word ant are the required one for the corresponding instruction execution.]

17. In regard to claim 25, Damouny in view of Thoma discloses the microprocessor of claim 1 wherein each of the plurality of embedded logic circuits comprises a table that performs a table lookup in response to a received instruction. [A PLA inherently uses a table. As reference to this inherency the Hennessy (Computer Architecture) textbook explicitly show on pages 105-206 that a PLA is table with entries for lookup. In addition, Hennessy (Computer Organization and Design) has shown on pages B-11 to B-13 that a PLA includes a pair of tables, and AND plane and an OR plane. These tables are used to perform table lookups because the inputs into the AND table are transformed into

intermediate values that fall down to the OR table and get further transformed into what results as the outputs.]

18. In regard to claim 26, Damouny in view of Thoma discloses the microprocessor of claim 25, wherein said controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup, [As shown in figure 1A of Damouny the branch PLA's are responsive to the control variable (element 184), the control signals for an immediately preceding instruction (element 182), and to the table lookup for setting the required control signals (element 183). The table use the control signals input to lookup the control signals to be output to element 156 via line 183.]

19. In regard to claim 27 Damouny in view of Thoma discloses the microprocessor of claim 23 wherein the controller includes means for maintaining a control signal at an immediately preceding value of said control signal. [As shown above, since control signals are set, they are kept up to date or maintained.]

20. In regard to claim 28, Damouny in view Thoma discloses the microprocessor of claim 27, wherein the controller includes:

a. means for setting a control signal to a "1" regardless of its immediately preceding value;

b. means for setting a control signal to a "0" regardless of its immediately preceding;

[Column 3, lines 14-17 show that the control signals are set to active high "1" and active low"0" . Since limitations (a) and (b) of the claim state that this setting is regardless of the preceding value and thus these limitations are met since all that is required is the setting of control signals to a "1" and to a "0".]

21. In regard to claim 29, Damouny in view of Thoma discloses the microprocessor of claim 28, wherein the controller further comprises means for setting a control signal to a data state. [As shown above, the control signals are set to active low or active high, a "0" or a "1" respectively. Since a "1" of "0" bit is data, the control is set to a data state.]

22. Claim 6, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damouny and Thoma as applied to claim 1 above, and further in view of Catherwoood (patent No. 5,457,802).

23. In regard to claim 6,30 Damouny discloses the microprocessor according to claim 1, further Damouny disclosed selectively modifying the value of the control signals where some value of some control signals are changed and others are remain the same value as discussed above. However Damouny did not expressly detail the determining of which control signal that are not to be modified for each instruction (claim 6) and means for determining at least one of said signals to be maintained for each instruction (claim 30). Catherwood however taught this limitations (e.g., see col. 3, lines 9-57)[Catherwood determines for specific instructions the signals that will be frozen in their previous state because these signal on "external conductors are not required by the

instruction. The reducing of the switching of reduces power requirements in the Catherwood system [Catherwood discloses the determination with and example instruction (RTS) that does not use external conductors (e.g., see col. 9, line 9-col. 11, line 63) and with an instruction (store,STA) that only uses external conductors for certain cycles (e.g., see col. 5, line 62-col. 7, line 43).

24. It would have been obvious to one of ordinary skill in the art to combine the teachings of Damouny and Catherwood. Both Damouny and Catherwood were directed toward the efficient processing of instructions on DP system comprising at least one integrated circuit processor operating as an embedded processor. One of ordinary skill would have been motivated to incorporate the Catherwood teaching of freezing the control signals to a previous value at least to reduce power requirement. The reduction of power requirements for computerized systems that are put in systems that use a limited source of power is a well known consideration for implementing embedded systems (e.g., see col. 1, line 15-col. 2, line 11 of Catherwood. Also Damouny taught use in embedded systems (e.g., see col. 1, line 50-col. 2, line 9).

Response to Arguments

25. The Examiner will address the arguments set forth in the appeal brief.

a) The Applicant argued in substance that disclosing generally that the pointers are necessary for execution does not mean that Damouny discloses or suggests setting only the required function signals and allegedly Damouny does not disclose suggest or even address the problems being solved by the claimed invention (claim 20). The Examiner contends that the claim 20 provides for

setting required function signals. The for an instruction to be operational it must set the "required function signals". So therefore inherently the signals shown in the Damouny reference that are set and described in the outstanding rejection comprise the required functions signals. Claim 20 provides for setting exclusive functions outside the current opcode to a previous state. Here Damouny taught that the function signals for the previous instruction are set or latched during the Processing of the current instruction as discussed in the outstanding rejection. Here for a previous instruction that is identical to the current instruction would inherently contain functions that differed at least partially from the functions of the Current instruction. Since Damouny taught setting or latching the previous instruction functions signals for the previous instruction during a current instructions then the is requires that the exclusive functions outside of the current opcode would have been set. The latching is taught by Damouny as discussed in the outstanding rejection. Claim 20 does not include any limitation that requires that only changing the value of signals that are absolutely required for a particular microcode address. Note there is no limitation as to which instruction(e.g., current or previous) (with exclusive functions outside the current opcode) are the exclusive functions included.

b) As to claim 1, Applicant alleges that claim 1 recites a microcode unit including a control signal for receiving all the control signals output by the microcode unit for an immediately preceding instruction. As to this limitation the claim 1, the Examiner contends that the claim only requires that for one (i.e., preceding) instruction all the control signals have to be input to the microcode

unit. The Damouny reference clearly disclosed that all the control signals required for a branch instruction was input to the microcode unit as discussed in the outstanding rejection. Here, as the branch control signals provide for the addressing a immediately succeeding instruction, the control signals for the branch (or immediately preceding instruction) is input to the microcode unit.

c) As to dependent claims 2-4, the modifying or setting of control signals to a "0" or "1" value regardless of its preceding value is discussed in the outstanding rejection. Note: for the limitation of means for not modifying a control signal from is its immediately preceding value. This claim limitation only requires that the value is not modified so if the system sets the same value for a signal of succeeding instruction to the same value a preceding instruction , the Examiner contends that the value has not been modified and therefore meets the claim limitation.

d) As to claim 6,30 the applicants arguments are moot because a new rejection is set forth above.

e) Applicant (with respect to claims 23-30) argues that (claim 24) The Damouny and Thoma disclosed a plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing the received instruction. The Examiner contends that Damouny and Thoma clearly shows as the opcode is decoded by a plurality of PLAs in parallel and only the signals from the selected PLA are output from the PLA for latching, setting and use by the system (see fig.1 of Thoma and the outstanding rejection above). Since the Thoma teaching of

selecting the functions by class provide then a smaller number of lines to specifiy a particular function then the intended use of limiting the number function signals that are set is indeed realizable. The Examiner contends the number of functions per class is specific the particular implementation and the limit of only one function to a some classes is not precluded by the Thoma teachings.

f) As per claim 27, Applicant alleges that Damouny did not disclose that the controller includes means for maintaining a control signal at an immediately preceding value of the control signal. The Examiner contends that the claim only requires that for one (i.e., preceding) instruction all the control signals have to be input to the microcode unit. The Damouny reference clearly disclosed that all the control signals required for a branch instruction was input to the microcode unit (as discussed in the outstanding rejection). Here, as the branch control signals provide for the addressing a immediately succeeding instruction, the control signals for the branch (or immediately preceding instruction) is input to the microcode unit (see fig. 1A of Damouny) Also as detailed in the outstanding rejection as the succeeding instruction is being processed the preceding instruction control signals are being set of latched.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ando (patent No. 5,497,496) disclosed a superscalar processor controlling fetching of instructions based upon number of empty instructions registers (e.g., see abstract and fig. 1).

Tinder (patent No. 5,063,536) disclosed a microprogrammable asynchronous controllers for digital electronic systems (e.g., see abstract).

Moyer (patent No. 6,119, 240) disclosed a low power data processing system for interfacing with an external device (e.g., see abstract).

Ando (patent No. 5,930,520) disclosed a pipelining device in a parallel processing apparatus and an instruction supplying method (e.g., see abstract).

Shau (patent No. 6,492,835) disclosed power saving methods for programmable logic arrays comprising storing results of previous PLA operation and bypassing a new operation if inputs are the same (e.g., see abstract).

Benayoun (patent No. 5,658,651) disclosed a hardware device for executing programmable instructions based upon micro-instructions (e.g., see abstract and fig. 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER